AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 10, line 6, and continuing to page 10, line 20, as follows:

Application related programs are run on the application processors 22, and are thus named in Fig. 4 as Application DSP #1 - Application DSP #N. In one mode of the invention illustrated in Fig. 4, each processor 22 has it's own multi-~~PHY~~ PHY address in the ATM switch port interface circuit 24. In this way it is possible to eliminate the need for all additional Mux/Demux logic schematically shown by dashed line box 26 in Fig. 4. This Mux/Demux logic could easily form a bottleneck in the system, especially when high speed data services are processed. The elimination of the Mux/Demux logic provides a significant advantage in the overall operation of the AMB. However, it should be understood that, in another mode of the invention, logic depicted by box 26 can be utilized consistent with the aspects of the invention, e.g., dynamic configuring of resources and functionalities. Usage of such the Mux/Demux logic in the form of a router is understood, e.g., with reference to United States Patent Application Serial No. 09/188,097, entitled "Centralized Queuing For ATM Node", filed November 9, 1998, which is incorporated herein by reference.

Please amend the paragraph beginning at page 10, line 26, and continuing to page 10, line 29, as follows:

Each of the application processors 22 has a Host Port Interface (HPI) 23. Each HPI 23 is connected to an external data memory space of the ~~EP~~ BP 28. The HPI is used mainly for the administration of the configuration operations of the AMB board 20 (loading or upgrading or amending of DSP software etc. operations).

Please amend the paragraph beginning at page 11, line 12, and continuing to page 11, line 21, as follows:

By replacing e.g. a router processor between each application processor 22 and the ATM Interface 24 a significant advantage is obtained by removing the limitations that this router (or similar) sets for the data processing capacity. In addition, by connecting each application processor 22 directly to its own UTOPIA Multi-PHY branch, the required bandwidth for interprocessor communication within the AMB is achieved independently of the physical location of the adjacent processor, which can be on the same ~~ANB~~ AMB or on another board in the same subrack, or even in another subrack or in another node of the system. Thus the granularity of the system can be in the application processor level rather than in the board level. This also makes it easier for the resource handler to manage the pooled objects in an optimal manner.

Please amend the paragraph beginning at page 13, line 9, and continuing to page 13, line 12, as follows:

- ALT board connected to a BSC or ~~ETS~~ BTS node. The ALT (ATM & AAL2 Link Termination) board is used for converting an AAL2' cell into AAL2 cells. The ALT board may also be used to prioritize the traffic in both ATM and in AAL2 levels.

Please amend the paragraph beginning at page 15, line 16, and continuing to page 15, line 32, as follows:

For example, if the BSC node of Fig. 7 detects that the number of mobile station (MS) to MS connections has increased in the system to an extent that more DHTs are needed, the main processor board (MPB 45) of BCS node ascertains whether there are any processors in the node which are spare or which could be converted from a prior functionality to a DHT functionality. In the situation of increased MS to MS connections, it is likely that less CODEC functionality is required at the BSC node. Therefore, the main processor board (MPB 45) determines that the CODEC functionality illustrated by one processor~~processors~~ 46 in Fig. 7 can be replaced by a DHT functionality. Therefore, as indicated by step 104 of Fig. 9 and depicted by arrow 49 in Fig. 7, the main processor board (MPB 45) downloads an applications module with DHT functionality to processor 46. In this regard, and as illustrated in Fig. 7, main processor board (MPB 45) has connected thereto a storage system 47 (such as a hard disk) which has stored thereon applications modules of differing functionality. For example, Fig. 7 shows that storage system 47 has DHT applications module 48a, CODEC module 48b, and PADP module 48n stored thereon. In the illustration herein described, the main processor board (MPB 45) downloads a copy of the DHT applications module 48a to replace the CODEC functionality at processor 46.